IN THE CLAIMS

The claims are not amended herein, but are presented for the Examiner's convenience.

1. (Previously Presented) A circuit for dividing an input clock signal into N clock signals having a relative phase separation of 360°/2N, where N is a positive integer, the circuit comprising:

a phase lock loop circuit receiving an input signal having a frequency F_0 and providing an output signal having a frequency $2NF_0$;

a Johnson counter having N JK flip-flops connected to receive as an input the output signal of the phase lock loop circuit and providing an output signal as an error signal to the phase lock loop circuit, said Johnson counter comprising an input JK flip-flop, an output JK flip-flop, and a plurality of middle JK flip-flops, each JK flip-flop having a J input, a K input, a clock input coupled to receive the output signal having the frequency $2NF_0$ from the phase lock loop circuit, a Q output, and a complemented Q output, each middle JK flip-flop and the output JK flip-flop having its J input coupled to the Q output of a preceding JK flip-flop and its K input coupled to the complemented Q output of the preceding JK flip-flop, the J input of the input JK flip-flop being coupled to the complemented Q output of the output JK flip-flop, and the K input of the input JK flip-flop being coupled to the Q output of the output JK flip-flop; and

said Johnson counter also being connected for providing at least two output signals from at least two of the N JK flip-flops of the Johnson counter as clock signals each having a phase displaced from the phase of the other 360/2N°.

2. (Original) The circuit of claim 1 wherein N =4.

3. (Original) The circuit of claim 1 wherein N=8.

4-19. (Canceled)

20. (Previously Presented) A method for generating at least two clock signals displaced from each other by a predetermined phase shift of 360°/2N, where N is a positive integer, the method comprising:

applying a clock signal to a signal input of a phase lock loop circuit at a desired clock frequency;

applying a feedback signal to a second input of the phase lock loop circuit;

generating an output signal of the phase lock loop circuit having a frequency of $2NF_0$;

coupling the output signal of the phase lock loop circuit to a clock input of each JK flip-flop of a Johnson counter to provide the feedback signal to the second input of the phase lock loop circuit having a frequency corresponding to the frequency of the output signal of the phase lock loop circuit divided by 2N, the Johnson counter comprising N JK flip-flops including an input JK flip-flop, an output JK flip-flop, and a plurality of middle JK flip-flops, each JK flip-flop having a J input, a K input, the clock input, a Q output, and a complemented Q output, each middle JK flip-flop and the output JK flip-flop having its J input coupled to the Q output of a preceding JK flip-flop and its K input coupled to the complemented Q output of the preceding JK flip-flop, the J input of the input JK flip-flop being coupled to the complemented Q output of the output JK flip-flop, the K input of the input JK flip-flop being coupled to the Q output of the output JK flip-flop; and

coupling outputs of the JK flip-flops of the Johnson counter for use as phase shifted clock outputs.

21. (Original) The method of claim 20 wherein N =4.

22. (Previously Presented) The circuit of claim 1 wherein the Johnson counter is coupled to provide a clock signal from each of the N JK flip-flops in response to the output signal having the frequency $2NF_0$, the error signal being one of the clock signals, the N clock signals having a relative phase separation of at least 360°/2N and each clock signal having a frequency F_0.

23. (Previously Presented) The circuit of claim 1 wherein the error signal and each clock signal has a frequency F_0.

24. (Previously Presented) The circuit of claim 1 wherein the phase lock loop circuit comprises:

a phase detector coupled to receive and compare the input signal having the frequency F_0 and the error signal from the Johnson counter and to provide an output signal corresponding to a phase difference between the input signal having the frequency F_0 and the error signal;

a low pass filter and a gain stage coupled to receive the output signal from the phase detector and to produce a control signal;

a voltage controlled oscillator coupled to the low pass filter and the gain stage to receive the control signal and coupled to the Johnson counter to produce the output signal having the frequency $2NF_0$ in response to the control signal.

25. (Canceled)

26. (Previously Presented) The circuit of claim 1 wherein each Q output and each complemented Q output of each JK flip-flop is coupled to provide a clock signal, the 2N clock signals having a relative phase separation of 360°/2N, and each clock signal having a frequency F_0.

27. (Previously Presented) The method of claim 20 wherein the feedback signal is one of the clock outputs, the clock outputs having a relative phase separation of at least 360°/2N and each clock output having a frequency F_0.

28. (Previously Presented) The method of claim 20, further comprising generating the feedback signal and each clock output with a frequency F_0.

29. (Previously Presented) The method of claim 20 wherein generating an output signal of the phase lock loop circuit comprises:

comparing the clock signal at the signal input and the feedback signal in a phase detector;

generating an output signal from the phase detector corresponding to a phase difference between the clock signal at the signal input and the feedback signal;

generating a control signal in a low pass filter and a gain stage in response to the output signal from the phase detector; and

generating the output signal of the phase lock loop circuit in response to the control signal in a voltage controlled oscillator coupled to the low pass filter and the gain stage.

30. (Canceled)

31. (Previously Presented) The method of claim 20, further comprising:

generating a clock output from each Q output and each complemented Q output of each JK flip-flop of the Johnson counter, the 2N clock outputs having a relative phase separation of 360°/2N, and each clock output having a frequency F_0.

32. (Previously Presented) A circuit to divide an input signal into multiple output clock signals, the circuit comprising:

a phase lock loop circuit coupled to receive an input signal having a frequency F_0 and coupled to provide an output signal having a frequency $2NF_0$, wherein N is a positive integer; and

a Johnson counter having N JK flip-flops coupled to receive as an input the output signal of the phase lock loop circuit and coupled to provide an output signal as an error signal to the phase lock loop circuit, the Johnson counter also being coupled to provide at least two output signals from at least two of the N JK flip-flops of the Johnson counter as output clock signals, each output clock signal having a phase displaced from a phase of each other output clock signal by at least 360/2N°, the Johnson counter comprising an input JK flip-flop, an output JK flip-flop,

and a plurality of middle JK flip-flops, each JK flip-flop having a J input, a K input, a clock input coupled to receive the output signal having the frequency $2NF_0$ from the phase lock loop circuit, a Q output, and a complemented Q output, each middle JK flip-flop and the output JK flip-flop having its J input coupled to the Q output of a preceding JK flip-flop and its K input coupled to the complemented Q output of the preceding JK flip-flop, the J input of the input JK flip-flop being coupled to the complemented Q output of the output JK flip-flop, and the K input of the input JK flip-flop being coupled to the Q output of the output JK flip-flop.

33. (Previously Presented) The circuit of claim 32 wherein N is 4.

34. (Previously Presented) The circuit of claim 32 wherein N is 8.

35. (Previously Presented) The circuit of claim 32 wherein the Johnson counter is coupled to provide an output clock signal from each of the N JK flip-flops in response to the output signal having the frequency $2NF_0$, the error signal being one of the output clock signals, the N output clock signals having a relative phase separation of at least 360°/2N and each output clock signal having a frequency F_0.

36. (Previously Presented) The circuit of claim 32 wherein the error signal and each output clock signal has a frequency F_0.

37. (Previously Presented) The circuit of claim 32 wherein the phase lock loop circuit comprises:

a phase detector coupled to receive and compare the input signal having the frequency F_0 and the error signal from the Johnson counter and to provide an output signal corresponding to a phase difference between the input signal having the frequency F_0 and the error signal;

a low pass filter and a gain stage coupled to receive the output signal from the phase detector and to produce a control signal;

a voltage controlled oscillator coupled to the low pass filter and the gain stage to receive the control signal and coupled to the Johnson counter to produce the output signal having the frequency $2NF_0$ in response to the control signal.

38. (Canceled)

39. (Previously Presented) The circuit of claim 32 wherein each Q output and each complemented Q output of each JK flip-flop is coupled to provide an output clock signal, the 2N output clock signals having a relative phase separation of 360°/2N, and each output clock signal having a frequency F_0.

40. (Previously Presented) A method of generating multiple output clock signals comprising:

applying an input clock signal having a frequency F_0 to a signal input of a phase lock loop circuit;

applying a feedback signal to an error input of the phase lock loop circuit;

generating an output signal having a frequency $2NF_0$ from the phase lock loop circuit wherein N is a positive integer;

coupling the output signal having the frequency $2NF_0$ from the phase lock loop circuit to a clock input of each JK flip-flop of a Johnson counter, the Johnson counter comprising N JK flip-flops including an input JK flip-flop, an output JK flip-flop, and a plurality of middle JK flip-flops, each JK flip-flop having a J input, a K input, the clock input, a Q output, and a complemented Q output, each middle JK flip-flop and the output JK flip-flop having its J input coupled to the Q output of a preceding JK flip-flop and its K input coupled to the complemented Q output of the preceding JK flip-flop, the J input of the input JK flip-flop being coupled to the complemented Q output of the output JK flip-flop, the K input of the input JK flip-flop being coupled to the Q output of the output JK flip-flop;

generating the feedback signal in the Johnson counter in response to the output signal having the frequency $2NF_0$ from the phase lock loop circuit; and

generating an output clock signal from at least two of the N JK flip-flops of the Johnson counter, each output clock signal having a phase displaced from a phase of each other output clock signal by at least 360/2N°.

41. (Previously Presented) The method of claim 40 wherein N is 4.

42. (Previously Presented) The method of claim 40 wherein N is 8.

43. (Previously Presented) The method of claim 40, further comprising generating an output clock signal from each of the N JK flip-flops of the Johnson counter, the feedback signal being one of the output clock signals, the N output clock signals having a relative phase separation of at least 360°/2N and each output clock signal having a frequency F_0.

44. (Previously Presented) The method of claim 40, further comprising generating the feedback signal and each output clock signal with a frequency F_0.

45. (Previously Presented) The method of claim 40 wherein generating an output signal having a frequency $2NF_0$ comprises:

comparing the input clock signal having the frequency F_0 and the feedback signal and in a phase detector;

generating an output signal from the phase detector corresponding to a phase difference between the input clock signal having the frequency F_0 and the feedback signal;

generating a control signal in a low pass filter and a gain stage in response to the output signal from the phase detector; and

generating the output signal having the frequency $2NF_0$ in response to the control signal in a voltage controlled oscillator coupled to the low pass filter and the gain stage.

46. (Canceled)

47. (Previously Presented) The method of claim 40, further comprising:

generating an output clock signal from each Q output and each complemented Q output of each JK flip-flop of the Johnson counter, the 2N output clock signals having a relative phase separation of 360°/2N, and each output clock signal having a frequency F_0.

48. (Previously Presented) The method of claim 20 wherein N =8